

Low-Voltage Differential Signaling (LVDS)

Design Notes

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Low-Voltage Differential Signaling (LVDS)

Introduction

Low-voltage differential signaling (LVDS) is a signaling method used for high-speed transmission of binary data over copper. It is well recognized that the benefits of balanced data transmission begin to outweigh the costs over single-ended techniques when signal transition times approach 10 ns. This represents signaling rates of about 30 Mbps or clock rates of 60 MHz (in single-edge clocking systems) and above.

LVDS, as documented in TIA/EIA-644, can have signal transition time as short as 260 ps turning a printed circuit board trace into a transmission line in a few centimeters. Care must be taken when designing with LVDS circuits, such as the SN65LVDS31 quadruple line driver and SN65LVDS32 quadruple line receiver. This document provides some guidelines for the basic application of LVDS.

System Definition

General Description

This application of LVDS in a data transmission system is one or more SN65LVDS31 transmitters and SN65LVDS32 receivers over 5 m of cable between the host and target controller. The host controller presents multiple bits of data prior to and after the clocking edge at a nominal 65 MHz rate. The cable consists of multiple twisted-pair signal cables, a power, and a ground wire with an overall shield and jacket. There are board-mounted connectors on the host and target printed circuit boards (PCBs).

System Diagram

Figure 1 shows a typical connection with LVDS transmitters and receivers.

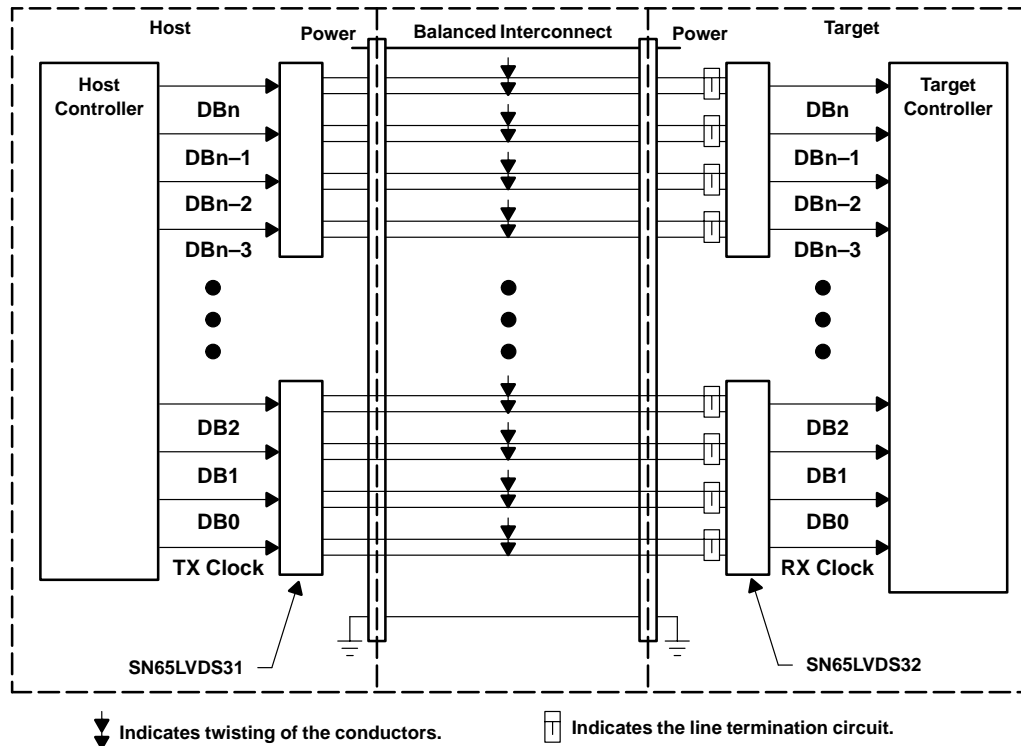


Figure 1. Typical Connection with LVDS Transmitters and Receivers

Interface Definition

The data inputs to the SN65LVDS31 are received at the interface of the PCB traces from the host controller and consist of up to n bits of information and a transmit (Tx) clock.

The data and clock signals are then transmitted differentially to the interface of the SN65LVDS31 outputs and interconnecting traces to the host PCB connector.

The signals then propagate from the interface of the host PCB connector and the cable connector and the balanced interconnecting media.

At the plug at the other end of the cable, the signals pass through the cable plug and target connector interface and then to the PCB traces of the target PCB.

The LVDS signal path ends at the interface of the target PCB traces and the termination circuit. There is an additional interface at the points where the PCB traces to the SN65LVDS32 inputs are connected.

The outputs of the receiver interface to the target PCB traces to the receiving controller.

Both the transmitter and receiver must be supplied with a reasonably clean nominal supply voltage of a 3.3 V and a connection to a ground plane.

Transmitter

Inputs

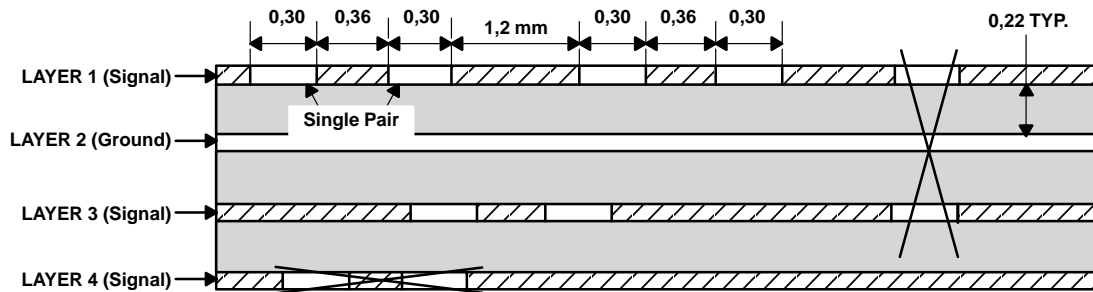
- Unused inputs to the SN65LVDS31 should be left open circuited. All inputs are internally pulled down to ground with approximately a 300-k Ω resistance.
- If not actively driven, the G (pin 4) or \overline{G} (pin 12) can be connected directly to V_{CC} or GND. Should a pull-up or pull-down resistor be used, a resistance of no more than 10 k Ω is recommended.
- The board trace between the host controller and the transmitter should be as short and matched in length as possible. With a 4-mA output buffer on the controller, keep the overall length of any trace run between the controller and transmitter less than 5 cm and all lengths matched to within 1 cm of each other. Longer lengths are possible with higher current output buffers.

Supply Voltage

- Place a 0.01- μ F Z5U ceramic, mica, or polystyrene dielectric 0805-size chip capacitor between pin 16 of the transmitter and the ground plane. The capacitor should be located as close as possible to the device pin.
- A ground plane is highly recommended, if not mandatory. A power plane is recommended, but if not used, sharing of supply traces with other components should be held to a minimum.

Outputs

- If the PCB trace is more than 2 cm in length between the transmitter output pins and the connector, the PCB must be constructed to maintain a controlled differential impedance near 100 Ω (see Figure 2).
- The physical length of each trace between the transmitter outputs and the connector should be matched to within 5 mm of each other. This usually requires mitering of the traces as shown in Figure 3.



- NOTES:
- A. All fabrication item must meet or exceed best industry practice.
 - B. Laminate material: copper clad FR-4
 - C. Copper weight: 1 oz. start
 - D. Finished board thickness: 0.032 (± 0.010) inches
 - E. Dielectric thickness to be symmetrical between all layers (± 0.005 inches)
 - F. Maximum warp and twist: 0.001 inches per inch
 - G. Circuitry on outer layers to be tin-lead plated (60/40), plated to 300 μin (minimum)
 - H. Soldermask both sides per artwork: green ethnone
 - I. Copper plating to be 0.001 inches (minimum) in plated-through holes
 - J. Soldermask over bare copper with tin-lead hot air leveling
 - K. Dimensions shown in Figure 2 are in millimeters

Figure 2. Typical PCB Construction

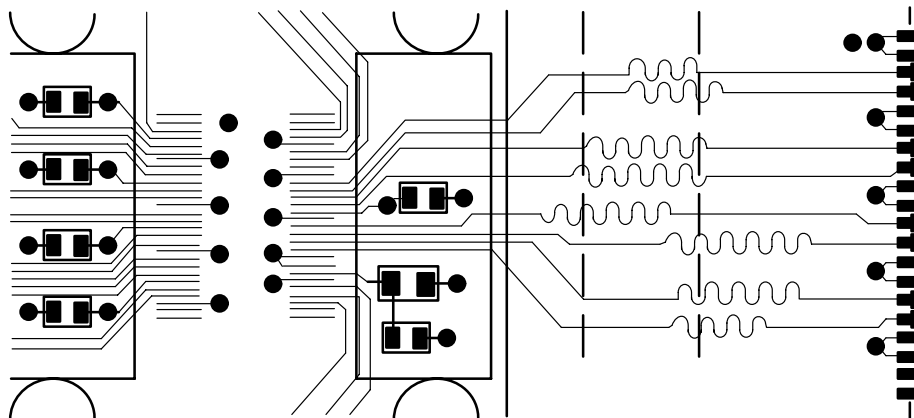


Figure 3. Mitering Output Traces to Closely Match Lengths

Receiver

Inputs

- If there is more than 2-cm distance between the connector and the receiver input pins, the PCB must be constructed to maintain a controlled differential impedance near 100 Ω .
- The physical length of each trace between the connector and the receiver inputs should be matched to within 5 mm of each other. This may require mitering of the traces.
- A common misconception is that the receiver requires a termination resistor. This is not true. Termination is part of the interconnection and may or may not be located at the inputs to the receiver. Please see the *Termination* section of this document for more details.
- The G (pin 4) or \bar{G} (pin 12) must be actively driven or connected directly to V_{CC} or GND through no more than a 10-k Ω resistance. There is no internal pull-up or pull-down resistance provided.

Supply Voltage

- Place a 0.01 μF Z5U ceramic, mica, or polystyrene dielectric 0805- or 0603-size chip capacitor between pin 16 and the ground plane. The capacitor should be located as close as possible to the device pin.

- A ground plane is highly recommended, if not mandatory. A power plane is recommended, but if not used, sharing of supply traces with other components should be held to a minimum.

Outputs

- The overall length of any board traces between the receiver outputs and the receiving controller should be as short and matched in length as possible. No run should be more than 5 cm long or 1 cm different from the others.
- The input capacitance to the controller should be less than 5 pF.

Interconnection

Characteristic Impedance

- At any cut point in the interconnect, the differential characteristic impedance should be 90 Ω to 130 Ω .
- Use polyethylene, polypropylene, or Teflon™ insulation in either round or flat cables and uniform distance between the conductors in a signal pair.
- Twisting of the signal pairs is recommended but not mandatory.
- Beldon #9807 is an example round cable.
- Beldon #9V28010 is an example flat cable.

Termination

- Termination at the far end of the interconnect from the transmitter is mandatory.
- The system diagram in Figure 1 shows locations of the terminations.
- The termination schematic diagram is shown in Figure 4.

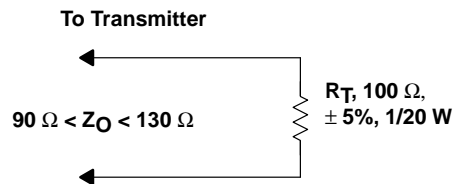


Figure 4. Differential Termination

- Use thick-film leadless (0603 or 0805) chip resistors.

Balance

- The distance and insulation between the signal and return conductors in a pair should be uniform.
- Any parasitic loading (capacitance) must be applied in equal amounts to each line.

Stubs

- A stub is any conductive path(s) connected to the cable conductors or PCB traces between the transmitter and receiver.
- A stub should be as short as possible but no longer than 2 cm to 3 cm.
- The interconnect ends at the termination. If the receiver cannot be located within 2 cm of the termination, use the fly-by termination shown in Figure 5.

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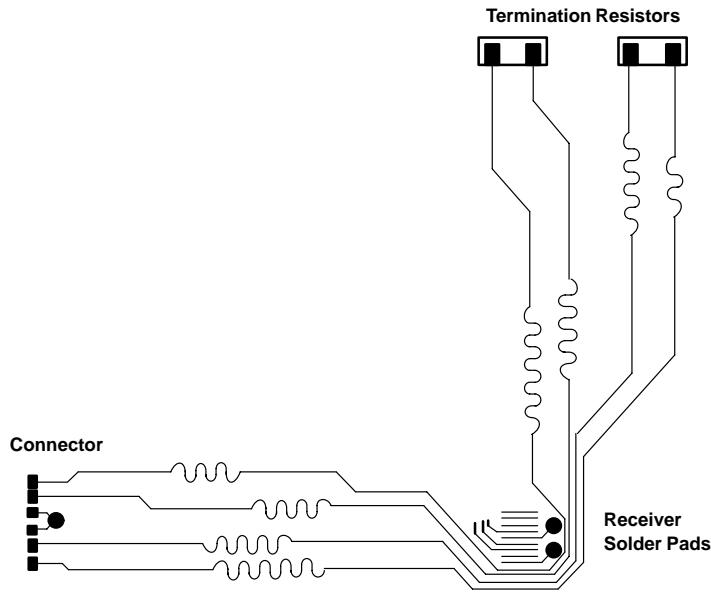


Figure 5. Fly-By Termination at the Receiver

Skew and ISI

- The maximum recommended cable length for non-encoded non-return to zero (NRZ) signaling is when the 10%-to-90% rise time of the signal at the termination is 8 ns for a 65 MHz clocked system. (The maximum recommended rise time for other clock rates may be calculated from $t_r < 1/[2f_{CLK}]$.)
- Keep the physical length of the signal pairs in the cable and PCB traces as close to the same as possible.
- The skew between signal pairs in good quality manufactured cables can range from 40 ps/m to 120 ps/m and should be specified by the vendor. A lower number is better.

Electromagnetic Compatibility

Electrostatic Discharge

- It is advisable that exposed connectors have pins recessed from the shell to prevent casual contact and discharges.
- It is also a good idea to have the ground pins longer than the signal pins in order to make the ground connection first and equalize the ground potentials before signal connections.

Radiated Emissions and Susceptibility

- There should be only one path for return current between the host controller and the target controller PCBs.
- Unused pins in connectors as well as unused wires in cables should be single-point grounded at the connector. Unused wires should be grounded at alternate ends.
- If an overall shield used, use a short pig-tail crimped to the shield end at each connector and then brought through a separate connector pin to a ground located as close to the connector as possible.
- If individual shielding of the signal pairs is used, use the same terminating technique as for the overall shield.